WHAT IS CLAIMED IS:

1. A wafer-level package comprising:

a semiconductor wafer having at least one semiconductor chip circuit forming region each including a semiconductor chip circuit and a plurality of chip terminals, said chip terminals including at least one test chip terminal and at least one non-test chip terminal;

at least one external connection terminal electrically connected to said at least one non-test chip terminal;

at least one redistribution trace provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out to a position offset from said one of said chip terminals;

at least one testing member provided in an outer region of said semiconductor chip circuit forming region, said second end of said redistribution trace being connected to said least one testing member; and

an insulating material covering at least said redistribution trace, said at least one external connection terminal and said at least one testing member being exposed from said insulating material.

2. The wafer-level package as claimed in claim 1, further comprising a sealing resin provided on said insulating material such that top parts of said

external connection terminals and said at least one testing member are exposed from said sealing resin.

3. The wafer-level package as claimed in claim 1, wherein said at least one external connection terminal and said at least one non-test terminal are electrically connected by an internal redistribution trace in such a manner that said at least one external connection terminal is provided at a position within said semiconductor chip circuit forming region and offset from said at least one non-test chip terminal.

4. The wafer-level package as claimed in claim 1, further comprising an excessive power supply protection element provided in said outer region and between said test chip terminal and said at least one testing member.

5. The wafer-level package as claimed in claim 1, wherein said at least one testing member includes at least one test terminal corresponding to said least one semiconductor chip circuit forming region, respectively, said test terminal being provided in said outer region.

6. The wafer-level package as claimed in claim 1, wherein said at least one testing member includes a plurality of test terminals corresponding to a plurality of said semiconductor chip circuit forming regions, respectively, and at least one common line connecting said test terminals, said test terminals and said common line being provided in said outer region.

7. The wafer-level package as claimed in claim 1, further comprising at least one common line provided in said outer region, a plurality of said redistribution traces extending out of a plurality of said semiconductor chip circuit forming regions being connected to said common line,

wherein said at least one testing member includes a test pad provided at a part of said common line and exposed from said insulating material.

8. The wafer-level package as claimed in claim 1, further comprising a plurality of units having different functions and provided within said semiconductor chip circuit forming region, a first end of said at least one redistribution trace being connected to one of, or combination of, said units, and a second end of said at least one redistribution trace being connected to said at least one testing member.

9. The wafer-level package as claimed in claim 1, further comprising a test-purpose circuit incorporated in said semiconductor chip circuit forming region, a first end of said at least one redistribution trace being connected to said test-purpose circuit and a second end of said at least one redistribution trace being connected to said at least one testing member.

10. The wafer-level package as claimed in claim 1, further comprising a test-purpose circuit provided in said outer region,

wherein said at least one testing member is provided on the test-purpose circuit or on the redistribution trace extending from the test-purpose circuit.

11. The wafer-level package as claimed in claim 1, further comprising:

a test history recording part provided in said outer region and connected to said second end of a plurality of said redistribution traces; and

input/output terminals for writing into/reading out from said test history recording part, said input/output terminals being exposed from said insulating material.

12. The wafer-level package as claimed in

claim 1, further comprising a common line in said outer region, a plurality of said redistribution traces extending out of a plurality of said semiconductor chip circuit forming region being connected to said common line,

wherein said at least one testing member includes a test supporting element provided at a part of said common line for testing said semiconductor chip circuit.

13. The wafer-level package as claimed in claim 1, wherein said at least one testing member includes a plurality of test terminals provided with a predetermined rule in such a manner that said semiconductor wafer can be identified from said positions of said test terminals.

14. A method of manufacturing a wafer-level package comprising the steps of:

a) preparing a semiconductor wafer having at least one semiconductor chip circuit forming region each provided with a semiconductor chip circuit and a plurality of chip terminals, at least one of said chip terminals being a test chip terminal and at least one being a non-test chip terminal;

b) providing a redistribution layer including an insulating film having through holes on the semiconductor wafer and an electrically conductive film formed on said insulating film, said film being formed into redistribution traces having a predetermined pattern;

c) providing external connection terminals and at least one testing member on said redistribution layer, said at least one testing member being provided at an outer region of said at least one semiconductor chip circuit forming region and connected to said test chip terminal via at least one of said redistribution traces; and

d) testing said at least one semiconductor chip circuit using said at least one testing member.

15. The method of manufacturing a wafer level package as claimed in claim 14, further comprising the step of:

e) providing a sealing resin on said redistribution layer in such a manner that top parts of said external connection terminals and said at least one testing member are exposed from said sealing resin.

16. A method of manufacturing a semiconductor device using a wafer-level package comprising the steps of:

a) manufacturing a wafer-level package including a semiconductor wafer having at least one semiconductor chip circuit forming region each including a semiconductor chip circuit and a plurality of chip terminals, said chip terminals including at least one test chip terminal and at least one non-test chip terminal;

at least one external connection terminal electrically connected to said at least one non-test chip terminal;

at least one redistribution trace provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out to a position offset from said one of said chip terminals; and

at least one testing member provided in an outer region of said semiconductor chip circuit forming region, said second end of said redistribution trace being connected to said at least one testing member,

b) testing said at least one semiconductor chip circuit provided in said at least one semiconductor chip circuit forming region using said at least one testing member; and

c) after said step b), cutting said wafer-level package along said outer region so as to manufacture at least one individualized semiconductor device.

17. The method of manufacturing a semiconductor device using a wafer-level package as claimed in claim 16, wherein in said step a), said external connection terminal and said at least one testing member are manufactured simultaneously.

18. The method of manufacturing a semiconductor device using a wafer-level package as claimed in claim 16, wherein in said step c), structures provided in said outer region, particularly said at least one testing member, are removed simultaneously.

19. A wafer-level semiconductor device comprising:

a semiconductor wafer having chip circuit forming regions;

at least one testing member provided in an outer region of the chip circuit forming regions; and

a line provided on the semiconductor wafer and connecting the at least one testing member and a test terminal provided in one of the chip circuit forming regions.

20. A semiconductor device comprising:

a semiconductor chip;

a test terminal and a non-test terminal provided to the semiconductor chip; and

a line which is connected to the test terminal and extends out of a circuit forming region.